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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,216	DISHONGH ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 October 2005 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 31-34, 36-38, 47-51, 53, 58, 59, and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by US 2001/0009066 A1 (Bhatt).

Bhatt discloses, referring to figure 12, a printed circuit board (PCB) comprising: a first signal routing layer (40) formed on a first surface of the PCB; an electrically conductive layer (40) (see ([0033]), at least one padless via (12, see [0008]) extending from the first signal routing layer to the electrically conductive layer, the at least one

padless via in electrical contact with the electrically conductive layer and a layer of solder mask material (50) formed over the first signal routing layer, the layer of solder mask material having at least one opening to expose the at least one padless via [claim 31], wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer [claim 32], further comprising a via plug (18) formed within the padless via [claim 33], further comprising a via plug (1wherein the via plug is formed of an electrically conductive material (18, see [0027]) [claim 34], wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane [claim 58].

Similarly, Bhatt discloses, referring to figure 12, a printed circuit board (PCB) comprising: a first signal routing layer (40) formed on a first surface of the PCB; at least one electrically conductive layer (40), and an array of interconnections formed on the first surface of the PCB, the array of interconnections including at least one padless via (12) extending from the first signal routing layer to the at least one electrically conductive layer, wherein the padless via is in electrical contact with the at least electrically conductive layer, [claims 36, 47], wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer (see [0033]) [claims 37, 48], further comprising an electrically conductive via plug (18) formed within the at least one padless via [claims 38, 51], wherein forming an array of interconnections on the first surface of the PCB comprises forming an array of

interconnection having an array pitch of 0.8mm or less (see [0025]) [claim 49], further comprising at least two conductive traces on the first signal routing layer between the at least on padless via and an adjacent interconnection [claim 50], wherein forming an array of interconnections on the first surface of the PCB comprises forming at least one contact pad on the first surface of the PCB adjacent to the at least on padless via, the at least one contact pad in electrical contact with a conductive trace on the first signal routing layer [claim 53], wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane [claims 59, 61].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 35, 41-44, 46, 52, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt in view of US 5,418,689 (Alpaugh).

Regarding claim 35, Bhatt discloses the claimed invention as described above with respect to claim 35 except, Bhatt does not specifically disclose a component attached to the PCB by a solder interconnection between a contact pad on a bottom surface of the component and the at least one padless via [claim 35]. However, it is well known in the art to attach components to PCB in this manner to vias as evidenced by Alpaugh (see col. 4, 50-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to attach a chip to the PCB in the invention of Bhatt. The motivation for doing so would have been to allow for signal processing.

Regarding claim 41, Bhatt discloses, referring to figure 12, a system comprising: a printed circuit board (PCB) including a first signal routing layer (40) formed on a first

surface of the PCB, at least one electrically conductive layer, and an array of interconnections formed on the first surface of the PCB, wherein the array of interconnections includes at least one padless via (12) extending from the first signal routing layer to the at least one electrically conductive layer, the at least one padless via electrically connected to the at least one electrically conductive layer. Bhatt does not specifically disclose a component attached to the PCB by a plurality of solder ball interconnections between the array of interconnections formed on the first surface of the PCB and a corresponding array of contact pads disposed on a bottom surface of the electronic component [claim 41]. However, it is well known in the art to attach components to PCB in this manner to vias as evidenced by Alpaugh (see col. 4, 50-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to attach a chip to the PCB in the invention of Bhatt. The motivation for doing so would have been to allow for signal processing.

Additionally, the modified invention of Bhatt teaches wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer [claim 42], further comprising at least two conductive traces on the first signal routing layer routed between the at least one padless via and an adjacent interconnection [claim 43], wherein the PCB is a motherboard and the component is a processor [claim 46], wherein forming a via plug within the at least one padless via comprises overplating the at least one padless via to form a via plug of plating material (see [0028]-[0030]) [claim 52], wherein the electrically conductive layer comprises a

conductive plane, and the at least one padless via is in electrical contact with the conductive plane [claim 60].

Furthermore, while the modified invention of Bhatt does not specifically teach that the width of the traces is approximately 3 mils [claim 44], instead generically teaching that the traces are "fine-line circuitry" ([0033]), it would have been obvious to one having ordinary skill in the art at the time of invention to make the width 3 mils. The motivation for doing so would have been to have been to provide a conductor of width sufficient to handle the require signal propagation, yet small enough to avoid wasting board space. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt in view of US 6,555,208 (Takada).

Regarding claim 39, Bhatt discloses the claimed invention as described above except Bhatt does not specifically state that contact pad is has a diameter of less than 18 mils [claim 39]. However, it is well known in the art to comprise contact pads in this size range as evidenced by Takada (see col. 16, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to make the pad in the invention of Bhatt less then 18 mils in diameter. The motivation for doing so would have been to reduce the footprint of the pad to allow for greater signal wiring

density. Moreover, it has been held that more than a mere change of form is necessary for patentability. Span-Deck, Inc v. Fab-con, Inc. (CA 8, 1982) 215 USPQ 835.

Similarly, regarding claim 40, Bhatt discloses the claimed invention as described above except Bhatt does not specifically state that the padless via has a diameter of 12 mils or less [claim 40]. However, it is well known in the art to comprise padless vias in this size range as evidenced by Takada (see col. 14, lines 20-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to make the padless via in the invention of Bhatt less then 12 mils in diameter. The motivation for doing so would have been to reduce the footprint of the pad to allow for greater signal wiring density. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt in view of Alpaugh as applied to claim 41 above, and further in view of Takada.

Regarding claim 45, the modified invention of Bhatt teaches the claimed invention as described above except the modified invention of Bhatt does not specifically state that contact pad is has a diameter of less than 18 mils [claim 45]. However, it is well known in the art to comprise contact pads in this size range as evidenced by Takada (see col. 16, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to make the pad in the modified invention of Bhatt less then 18 mils in diameter. The motivation for doing so

would have been to reduce the footprint of the pad to allow for greater signal wiring density. Moreover, it has been held that more than a mere change of form is necessary for patentability. Span-Deck, Inc v. Fab-con, Inc. (CA 8, 1982) 215 USPQ 835.

Claims 54-57 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,521,846 B1 (Freda) in view of Bhatt.

Freda discloses, a method of attaching a component to a printed circuit board (PCB) comprising: aligning solder balls (11) attached to an array of contact pads on a bottom surface of the component with a corresponding array of interconnections (21) formed on a first surface of the PCB, the array of interconnections comprising at least one via (22) extending from a first signal routing layer on the first surface of the PCB to an electrically conductive layer (24), wherein the at least one via is in electrical contact with the electrically conductive layer; and reflowing the solder balls to electrically connect the array of contact pads to the corresponding array of interconnections. Freda does not specifically state that the via is padless [claim 54]. However, it is well known in the art to use padless vias in PCB as evidenced by Bhatt (see [0008]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a padless via as is known in the art and evidenced by Bhatt as the via in the invention of Freda. The motivation for doing so would have been to reduce the spaced

required of the via and provide the opportunity of increased wiring density (Bhatt [0008]).

Additionally, the modified invention of Freda teaches, wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer [claim 55], wherein the component is an LGA socket (see col. 3, lines 60-65) [claim 57], wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane [claim 62].

Also, regarding claims 56, although the modified invention of Freda does not specifically teach that the BGA has a pitch of 0.8mm or less [claim 56], less a modification would have bee trivial to the ordinarily skilled artisan. The motivation for doing so would have been to choose a pith wide enough to avoid short circuits yet small enough to reduce the footprint of the device, thus freeing up premium board space for additional wiring. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Response to Arguments

Applicant's arguments with respect to claims 31-62 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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